

REMARKS

Claims 1-7, 14, 15 and 21-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner, *et al.* (U.S. Patent Number 5,882,973) in view of Nguyen (U.S. Patent Number 6,472,261) and Huang (U.S. Patent Number 5,899,722). In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

The claims are amended to clarify features of the applicants' claimed semiconductor device. It is believed that these claim amendments clarify the patentable distinctions between the applicants' invention and the cited combination of references. Specifically, the claims are amended to clarify the applicants' first insulation layer and second conductive layer such that the cited combination of references fails to teach or suggest the invention set forth in the amended claims.

The applicants' claimed first insulation layer 8, 28, 50, 70, 90 is a relatively thick flat layer through which the applicants' claimed conductive patterns 4 and 6, 24 and 26, 44 and 46, 64 and 66, and 84 and 86, as well as the applicants' claimed contact portion of a second conductive layer 16, 34, 56, 76 and 96 are formed. Since the conductive patterns and the contact portion of the second conductive layer are formed in the first insulating layer, the first insulating layer substantially fills the gaps between these layers. This is in contrast to other structures in which an insulating layer may be conformally coated or formed on conductive layers. The gap filling characteristics of the applicants' first insulation layer are set forth in the claims by reciting

that the first insulation layer has portions that extend between adjacent conductive patterns and between the contact portion of the second conductive layer and the conductive patterns, and that these portions of the first insulation layer have a top surface that is substantially planar and has a substantially constant height.

The portion of Gardner, *et al.*'s etch stop layer 26 underneath Gardner, *et al.*'s spacer 28b, cited by the Examiner as the applicants' claimed first insulation layer, is not the first insulation layer claimed by the applicants. Specifically, the portion of the etch stop layer 26 underneath the spacer 28b in Gardner, *et al.* does not fill gaps between adjacent conductive patterns, as set forth in the amended claims, nor does it have portions that extend between adjacent conductive patterns and between a contact portion of the second conductive layer and conductive patterns. That is, there is no portion of Gardner, *et al.*'s silicide 48 that is higher than any portion of Gardner, *et al.*'s gate electrodes 18a and 18b.

To further clarify the gap-filling nature of the applicants' claimed first insulation layer, the claims are further amended to set forth that the top surface of the first insulation layer is higher than a bottom surface of the conductive patterns. In contrast to this claim language, in Gardner, *et al.*, the portion of the etch stop layer 26 beneath the spacer 28b does not have a top surface above the bottom surface of the gate electrodes 18a and 18b. This is clear because the gate electrodes 18a and 18b are formed on top of the etch stop layer 26.

The claims are further amended to clarify the structure of the contact portion of the second conductive layer such that the distinctions between the applicants' second conductive layer and that shown in the cited prior art are clarified. Specifically, the claims are amended to specify that the contact portion of the second conductive layer is laterally between adjacent conductive patterns. That is, there is at least a portion of the contact portion of the second conductive layer that is at the same height as at least a portion of the conductive patterns. This clearly distinguishes a structure such as that shown in Gardner, *et al.* in which the silicide layer 48, cited by the Examiner as the applicants' claimed second conductive layer, is not laterally adjacent to gate conductors 18a and 18b, cited by the Examiner as the applicants' claimed plurality of conductive patterns. Instead, the silicide layer 48 of Gardner, *et al.* is at a lower level than the gate conductors 18a and 18b.

In summary, the applicants' first insulation layer set forth in the amended claims is clearly distinguished from the portion of an etch stop layer 26 formed under a spacer 28b disclosed by Gardner, *et al.* Likewise, the applicants' second conductive layer set forth in the amended claims is distinguished from the silicide layer 48 in Gardner, *et al.*

In the Office Action, it is stated that Nguyen teaches a semiconductor device having a self-aligned contact. Huang is cited as teaching a conductive layer being a single uninterrupted layer formed over conductive patterns and having a contact portion that fills a contact hole. However, even if one were to add the plug 42 of Nguyen and the polysilicon layer 17 of Huang to the structure of Gardner, *et al.*, the invention set forth in the amended claims does not result.

Specifically, there is no combination of the references which would result in teaching or suggesting the applicants' first insulation layer and second conductive layer. Specifically, in Gardner, *et al.*, the portion of the etch stop layer 26 beneath the spacers 28b is formed at a level lower than the gate electrodes 18a, 18b, since the gate electrodes are formed on top of the etch stop layer 26. Furthermore, the thermal oxide layer 22 of Nguyen is a conformal layer and does not have a single substantially planar top surface having a substantially constant height. Likewise, in Huang, there is neither taught nor suggested an insulation layer that fills gaps between adjacent conductive patterns and between conductive patterns and a contact portion of a second conductive layer, as set forth in the amended claims.

Accordingly, there is no way to combine the cited Gardner, *et al.*, Nguyen and Huang references to teach or suggest the invention set forth in the amended claims in which a first insulation layer fills gaps between conductive patterns and has a single substantially planar top surface that has a constant height between conductive patterns and a second conductive layer and that is higher than a bottom surface of the conductive patterns. Furthermore, there is no way to combine the cited references to obtain the applicants' claimed second conductive layer in combination with the claimed first insulation layer, in which at least a portion of the contact portion of the second conductive layer is laterally adjacent to the conductive patterns such that the portion of the contact portion of the second conductive layer is higher than a bottom surface of the conductive patterns, as set forth in the amended claims.


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Accordingly, it is believed that the claims are allowable over the cited references, and, therefore, reconsideration of the rejections of claims 1-7, 14, 15 and 21-40 under 35 U.S.C. § 103(a) based on Gardner, *et al.*, Nguyen and Huang is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that, upon entry of this Amendment, all claims pending in the application will be in condition for allowance. Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

Date: 3/10/05
Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
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Steven M. Mills
Registration Number 36,610
Attorney for Applicants